What is claimed is:

1. An ATM adaptation layer apparatus, comprising:

an ATM adaptation layer processor connected to an external Utopia level 2 matching device for processing and outputting a virtual path and a virtual channel of input/output cell data;

an ATM routing processor having one end connected to the ATM adaptation layer processor and the other end connected to an external ATM switch for processing a routing path of the input cell data; and

a controller for downloading program data from outside, generating corresponding control signals, and outputting data on a communicating status to outside.

2. The ATM adaptation layer apparatus of claim 1, wherein the ATM adaptation layer processor comprises:

a first SRAM, on which a virtual channel and a virtual path address of the cell data inputted from the external Utopia level 2 matching section are loaded; and

a second SRAM, on which a virtual channel and a virtual path address of the cell data outputted to the external ATM switch are loaded.

3. The ATM adaptation layer apparatus of claim 1, wherein the ATM adaptation layer processor further comprises a first clock generator provided at one end thereof for

generating a first clock, and a clock driver provided at the other end thereof for transferring the first clock signal of the first clock generator to the ATM adaptation layer processor.